CLAIMS

What is claimed is:

1. A method of designing a programmable logic device comprising the steps of:

receiving a modification to a programmable logic device that has been floorplanned;

identifying modules of the programmable logic device that have been changed by the modification;

floorplanning only the changed modules thereby determining a placement solution that does not violate boundaries of the unchanged modules; and

placing and routing the programmable logic device.

2. The method of claim 1, said floorplanning step further comprising:

selecting a shape from a set of shapes for each changed module; and

assigning each changed module a non-overlapping location on the programmable logic device according to the selected shape of each module.

3. The method of claim 2, further comprising generating shapes for each changed module.

4. The method of claim 2, said floorplanning step further comprising adjusting a boundary of one of the changed modules to accommodate at least one component of the module without violating a boundary of an unchanged module.

5. The method of claim 1, wherein the programmable logic device is a field programmable gate array.

6. The method of claim 1, wherein the modification does not alter more than approximately 5 percent of the components of a module.

7. The method of claim 1, wherein the modification does not alter more than approximately 10 percent of the components of a module.

8. A system for designing a programmable logic device comprising:

means for receiving a modification to a programmable logic device that has been floorplanned;

means for identifying modules of the programmable logic device that have been changed by the modification;

means for floorplanning only the changed modules thereby determining a placement solution that does not violate boundaries of the unchanged modules; and

means for placing and routing the programmable logic device.

9. The system of claim 8, said means for floorplanning further comprising:

means for selecting a shape from a set of shapes for each changed module; and

means for assigning each changed module a non-overlapping location on the programmable logic device according to the selected shape of each module.

10. The system of claim 9, further comprising means for generating the set of shapes for the changed modules.

11. The system of claim 9, said means for floorplanning further comprising means for adjusting a boundary of one of the changed modules to accommodate at least one component of the module without violating a boundary of an unchanged module.

12. The system of claim 8, wherein the programmable logic device is a field programmable gate array.

13. The system of claim 8, wherein the modification does not alter more than approximately 5 percent of the components of a module.

14. The system of claim 8, wherein the modification does not alter more than approximately 10 percent of the components of a module.

15. A machine readable storage, having stored thereon a computer program having a plurality of code sections executable by a machine for causing the machine to perform the steps of:

receiving a modification to a programmable logic device that has been floorplanned;

identifying modules of the programmable logic device that have been changed by the modification;

floorplanning only the changed modules thereby determining a placement solution that does not violate boundaries of the unchanged modules; and

placing and routing the programmable logic device.

16. The machine readable storage of claim 15, said floorplanning step further comprising:

selecting a shape from a set of shapes for each changed module; and

assigning each changed module a non-overlapping location on the programmable logic device according to the selected shape of each module.

17. The machine readable storage of claim 16, further comprising generating shapes for each changed module.

18. The machine readable storage of claim 16, said floorplanning step further comprising adjusting a boundary of one of the changed modules to accommodate at least one component of the module without violating a boundary of an unchanged module.

19. The machine readable storage of claim 15, wherein the programmable logic device is a field programmable gate array.

20. The machine readable storage of claim 15, wherein the modification does not alter more than approximately 5 percent of the components of a module.

21. The machine readable storage of claim 15, wherein the modification does not alter more than approximately 10 percent of the components of a module.